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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,771	06/23/2003	Norio Ishitsuka	500.42877X00	5732

20457 7590 03/08/2005

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EXAMINER	
TSAI, H JEY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,771	ISHITSUKA ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *12-44,47 and 48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,45 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restriction

Applicant's election of claims 1-11 and 45-46 of species 1 is acknowledged.

This application contains claims drawn to an invention nonelected with traverse. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Specification/Drawings

The substitute specification and replacement sheets of drawings filed on August 2, 2004 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 10-11 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang 6,406,987, previously applied, in view of Huang 6,235,606, newly cited.

Huang discloses a semiconductor device, which includes :

semiconductor substrate 1, fig. 6-7 and col. 4, lines 49+,

an element isolating region 12 having a trench (STI) formed in said semiconductor substrate 1 and an embedding insulating film 12 which is embedded into the trench (STI),

an active region formed adjacent to the element isolating region 12, in which gate insulating 14 film is formed,

a gate electrode 16 is formed on the gate insulating film 14, col. 5, lines 4+,

a region formed in such a manner that at least a portion of the gate electrode 16 positioned on the element isolating region 12 (fig. 7), and first edge surface of an upper side of embedding insulating film 12 in a first element isolating region (left hand side of fig. 7) where gate electrode is positioned at a vertically higher plane than a second edge surface of the embedding insulating film in a second element isolating region where said gate electrode film 16 (left hand side of fig. 7) is not positioned,

second edge surface is 500-1000 angstroms which is greater than the gate oxide of 40 angstroms, col. 5, lines 52+,

active region has impurity doped region 17/18,

a boundary plane (A),

an interlayer insulating film 21, fig. 8.

The difference between the references applied above and the instant claim(s) is: Huang '987 teaches forming a CMOS but does not teaches that CMOS device including a well region. However, Huang '606 teaches at fig. 1E, 2E, source/drain region 120 formed in the well region 116. Since, source/drain region counter dopes the well region to form opposite conductivity region, hence, it obvious that doping density of source/drain region of n-type is has a higher doping density of well region

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by forming transistor in the well region as taught by Hung '606 because both n and p types transistor can be formed in the same substrate for a CMOS device.

Claim 9 is rejected under 35 U.S.C 103 as being unpatentable over Huang as applied to claims 1-8, 10-11 and 45-46 above, and further in view of Nishioka 2002/0008019, previously applied.

The difference between the references applied above and the instant claim(s) is: Huang teaches an embedding oxide film but does not specify the oxide is a HDP oxide. However, Nishioka teaches at para. 6, an embedding oxide film is a HDP oxide. And, the selection of oxide density and coating thickness as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings with HDP oxide as taught by Nishioka because higher density of oxide increases the insulation value.

Claims 1- 8, 10-11 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee 6,184,071, in view of Huang 6,235,606 both are newly cited.

Lee discloses a semiconductor device, which includes:

semiconductor substrate 1, fig. 2A-2B and col. 4, lines 10-67,

an element isolating region 39 having a trench formed in said semiconductor substrate 1 and an embedding insulating film 39 which is embedded into the trench,

an active region formed adjacent to the element isolating region 39, in which gate insulating 14 film is formed,

a gate electrode 41 is formed on the gate insulating film,

a region formed in such a manner that at least a portion of the gate electrode 41 positioned on the element isolating region 39, and first edge surface of an upper side of embedding insulating film 39 in a first element isolating region where gate electrode 41 positioned is positioned at a vertically higher plane than a second edge surface the embedding insulating film in a second element isolating region where said gate electrode film 41 is not positioned,

active region has impurity doped region 43,

a boundary plane (A),

an interlayer insulating film 45.

The difference between the references applied above and the instant claim(s) is: Lee does not teach that substrate includes a well region. However, Huang '606 teaches at fig. 1E, 2E, source/drain region 120 formed in the well region 116. Since, source/drain region counter dopes the well region to form opposite conductivity region, hence, it obvious that doping density of source/drain region of n-type is has a higher doping density of well region. And, the selection of coating thickness as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by forming transistor in the well region as taught by Hung '606 because both n and p types transistor can be formed in the same substrate for a CMOS device.

Claim 9 is rejected under 35 U.S.C 103 as being unpatentable over Lee as applied to claims 1-8, 10-11, 45-46 above, and further in view of Nishioka 2002/0008019, previously cited.

The difference between the references applied above and the instant claim(s) is: Lee teaches an embedding oxide film but does not specify the oxide is a HDP oxide. However, Nishioka teaches at para. 6, an embedding oxide film is a HDP oxide. And, the selection of oxide density and coating thickness as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine

experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings with HDP oxide as taught by Nishioka because higher density of oxide increases the insulation value.

Applicant's arguments filed on 7/23/04, 8/2/04, 11/24/04 have been fully considered but they are not persuasive. Because Huang '987 clearly teaches first edge surface of an upper side of embedding insulating film 12 in a first element isolating region (left hand side of fig. 7) where gate electrode positioned is positioned at a vertically higher plane than a second edge surface of the **embedding insulating film** in a second element isolating region where said gate electrode film 16 (left hand side of fig. 7) is not positioned. Even though Huang teaches a visor 20' formed over the embedding insulating layer 12, Huang's gate electrode is still formed higher than a second edge surface of the embedding insulating film 12 as claimed. Newly cited reference, Lee also clearly teaches a region formed in such a manner that at least a portion of the gate electrode 41 positioned on the element isolating region 39, and first edge surface of an upper side of embedding insulating film 39 in a first element isolating region where gate electrode 41 is positioned at a vertically higher plane than a second edge surface the embedding insulating film in a second element isolating region where said gate electrode film 41 is not positioned as set forth above.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

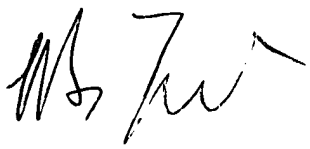
Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the Group customer service whose telephone number is (703) 306-3329 and Fax number (703) 872-9306. Group receptionist telephone number 703-308-0956.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebenttri can be reached on (571) 272-1673. The fax phone number for this Group is (703) 872-9306.

hjt

1/31/2005



H. Jey Tsai
Primary Examiner
Patent Examining Group 2800